UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/177,572	10/23/1998	YOSHIHIRO TERASHIMA	35.C13035	3325

5514 7590 05/22/2002

FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER
NGUYEN, KEVIN M

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 05/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/177,572	Applicant(s) TERASHIMA ET AL.	
	Examiner Kevin M. Nguyen	Art Unit 2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 March 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. The amendment filed on 3/13/2002 is entered. The rejections of claims 13-16 are maintained.

Claim Objections

2. Claims 13 and 15 are objected to because of the following informalities: SDRAM and FIFO are undefined. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki (US 4,745,485) in view of Ebihara et al hereinafter Ebihara (US 4,864,402), and further in view of Kelleber (US 5,794,016).

6. As to claim 13, Iwasaki teaches a memory controller which includes data signal input from the S/P converter 2 converts the serial video signal to a parallel signal for every eight bits. The parallel video signal converted by the S/P converter 2 is supplied to a latch circuit 3 (first FIFO memory). The latch circuit 3 (FIFO3) is supplied to frame memories 4 and 5 serve to store for one frame (col. 3, line 29), a latch circuit 6 (second memory) for the data read out (see figure 1, column 3, lines 18-29). The picture element data is displayed with good quality on the liquid crystal display (10) by using the frame memories (4 and 5) corresponding to one frame (see abstract). Therefore, Iwasaki teaches all of the claimed limitations of claim 13, except for "a frame merry having a capacity of a single frame, a continuous period of writing into and reading from said frame memory is designed as an L cycle, a single time of continuous writing period and two times of continuous reading period are performed during a period N*L....." However, Ebihara teaches a related video memory having positively a single memory structure (see col. 3, lines 26-30), the output data is supplied through the multiplier 5 to the adder 3 thereby to form a kind of cyclic-type filter (a continuous period of writing into and reading from said frame memory is designed as a L cycle, col. 5, lines 49-51), a write address signal circuit 13, first read address signal circuit 14, and a second read address signal circuit 14A (see Fig. 5), the read address signal is higher than the write address signal in frequency with a shorter cycle (an instruction period instructing the memory necessary for performing continuous access to the frame memory is shorter than a remaining period, col. 2, lines 56-57). It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the additional video memory

taught by Ebihara in the memory controller of Iwasaki's LCD system in order to improve the quality of picture while achieving the functions of a time base corrector, a noise reducer and a comb filter by a single memory structure without making the peripheral circuit complicated (see col. 3, lines 25-34 of Ehihara). Therefore, Iwasaki and Ebihara fail to teach synchronous dynamic random access memory SDRAM. However, Kelleher teaches the graphics memory 22 having four 1Mx16 SDRAMs (figure 1), eight 1Mx16 SDRAMs (figure 2), sixteen 1Mx16 SDRAMs are used to construct a thirty-two Mbytes graphics memory system 22 (col. 4, lines 31-39). It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate the plurality of SDRAMs 22 taught by Kelleher for the frame memory 4 and of Iwasaki's and DRAM 12 of Ebihara's system because this would provide a parallel graphics architecture appropriate graphics workstations that is scalable to the needs of a user (col. 1, lines 6-9 of Kelleher).

7. As to claim 14, Iwasaki teaches the driver 9 drives the liquid crystal display 10 (see Fig. 1, column 3, lines 51-52).

8. As to claim 15, Iwasaki teaches a memory controller which includes data signal input from the S/P converter 2 converts the serial video signal to a parallel signal for every eight bits. The parallel video signal converted by the S/P converter 2 is supplied to a latch circuit 3 (first FIFO memory). The latch circuit 3 (FIFO3) is supplied to frame memories 4 and 5 serve to store for one frame (col. 3, line 29), a latch circuit 6 (second memory) for the data read out (see figure 1, column 3, lines 18-29). The picture element data is displayed with good quality on the liquid crystal display (10) by using the frame

memories (4 and 5) corresponding to one frame (see abstract). Therefore, Iwasaki teaches all of the claimed limitations of claim 13, except for "a frame memory having a capacity of a single frame, a continuous period of writing into and reading from said frame memory is designed as an L cycle, a single time of continuous writing period and two times of continuous reading period are performed during a period N*L....." However, Ebihara teaches a related video memory having positively a single memory structure (see col. 3, lines 26-30), the output data is supplied through the multiplier 5 to the adder 3 thereby to form a kind of cyclic-type filter (a continuous period of writing into and reading from said frame memory is designed as a L cycle, col. 5, lines 49-51), a write address signal circuit 13, first read address signal circuit 14, and a second read address signal circuit 14A (see Fig. 5), the read address signal is higher than the write address signal in frequency with a shorter cycle (an instruction period instructing the memory necessary for performing continuous access to the frame memory is shorter than a remaining period, col. 2, lines 56-57), the frame delay circuit 4 operates at low speed (see col. 1, lines 33-34). It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the additional video memory taught by Ebihara in the memory controller of Iwasaki's LCD system in order to improve the quality of picture while achieving the functions of a time base corrector, a noise reducer and a comb filter by a single memory structure without making the peripheral circuit complicated (see col. 3, lines 25-34 of Ehihara). Therefore, Iwasaki and Ebihara fail to teach synchronous dynamic random access memory SDRAM. However, Kelleher teaches the graphics memory 22 having four 1Mx16 SDRAMs (figure 1), eight 1Mx16

SDRAMs (figure 2), sixteen 1Mx16 SDRAMs are used to construct a thirty-two Mbytes graphics memory system 22 (col. 4, lines 31-39). It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate the plurality of SDRAMs 22 taught by Kelleher for the frame memory 4 and of Iwasaki's and DRAM 12 of Ebihara's system because this would provide a parallel graphics architecture appropriate graphics workstations that is scalable to the needs of a user (col. 1, lines 6-9 of Kelleher).

9. As to claim 16, Iwasaki teaches the driver 9 drives the liquid crystal display 10 (see Fig. 1, column 3, lines 51-52).

Response to Arguments

10. Applicants argues that in claim 13 recites "a SDRAM having a capacity of a single frame for reading data at the same frequency as the input frequency of the input data after storing a predetermined quantity, a*N*L bits... a second FIFO memory having width a*N for reading from a SDRAM at the same frequency as the input data and for storing temporarily the data, such that, after storing data of a predetermined quantity 2*a*N*L into a second FIFO memory...." This argument are not persuasive because Kelleher's invention teaches the graphics memory 22 having four 1Mx16 SDRAMs (figure 1), eight 1Mx16 SDRAMs (figure 2), sixteen 1Mx16 SDRAMs are used to construct a thirty-two Mbytes graphics memory system 22 (col. 4, lines 31-39). These arguments are not persuasive because it would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate the plurality of SDRAMs 22 taught by Kelleher for the frame memory 4 and of Iwasaki's and DRAM 12

of Ebihara's system because this would provide a parallel graphics architecture appropriate graphics workstations that is scalable to the needs of a user (col. 1, lines 6-9 of Kelleher).

For these reasons, the rejections of claims 13-16 based on Iwasaki, Ebihara et al, and Kelleher are maintained.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kevin M. Nguyen** whose telephone number is **703-305-6209**. The examiner can normally be reached on M-F (9:00-5:00), with alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard Hjerpe** can be reached on **703-305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Kevin M. Nguyen
Examiner
Art Unit 2674

ULKA J. CHAUHAN
PRIMARY EXAMINER